Amendments to the Specification

Please replace the paragraph beginning on page 3, line 7, with the following rewritten paragraph:

During a read operation of an MRAM array, data may be read from a magnetic cell junction by creating a current path from a corresponding bit line through the magnetic cell junction to an underlying transistor such that a resistance measurement may be obtained. The underlying transistor may be turned "on" by the application of a bias voltage. In general, the resistance measured through a magnetic cell junction may be a function of the applied bias voltage. Variations within magnetic cell ~~junction~~ junctions may, however, cause the level of bias voltage attributed to a maximum sense signal to vary from cell to cell as well as from die to die and wafer to wafer. Consequently, the determination of an optimum bias voltage may be difficult in some embodiments. In addition, variations within magnetic cell junctions may cause a breakdown voltage of a magnetic cell junction to be low in some embodiments. Low breakdown voltages may, in some cases, cause read failures, reducing the reliability of the device. In general, a breakdown voltage of a magnetic cell junction may decrease with time. As such, an MRAM array may function properly during testing, but may, in some cases, fail at a later point in time, resulting in unpredictable reliability.

Please replace the paragraph beginning on page 19, line 1, with the following rewritten paragraph:

As used herein, the reference of a north bit line and a south bit line for pulse generators 22 and ~~46~~ 58 may refer to the opposing ends of a bit line to which current may be applied such that current applications through the bit line are bi-directional. As such, north bit line pulse generator 22 may include circuitry by which to generate current along one direction of a bit line and south bit line pulse generator 58 may include circuitry by which to generate current along the other direction of the bit line. Exemplary circuits that may used for north bit line pulse generator 22 and south bit line pulse generator 58 are illustrated in Fig. 6. Other configurations of circuits, however, may be used for the bit line generators, depending on the design specifications of the device. As such, north bit line pulse generator 22 and south bit line pulse generator 58 are not necessarily restricted to the circuitry illustrated and described in reference to Fig. 6.

Please replace the paragraph beginning on page 21, line 1, with the following rewritten paragraph:

In some cases, the circuitry used to alter current applications along the bit and/or digit lines of MRAM device 10 may be used to identify "errant" magnetic elements. In particular, during the course of altering current along the bit and/or digit lines of the device, errant magnetic elements, such as selected cells which ~~are~~ require too large of a current to switch their magnetization or disturbed cells which change their magnetization at a low current level, may be detected. Such errant magnetic elements may be discarded and, in some embodiments, replaced, improving the reliability of the device. In general, the circuitry used to alter current applications of current to magnetic memory arrays 12 to identify errant elements, create a probability switching distribution and/or determine an optimum programming current may include any one or combination of circuitry included in adjustable pulse delay 16, adjustable pulse width 20, program pulse timing generator 18, north bit line pulse generator 22, south bit line pulse generator 58, digit line pulse generator 56 and/or adjustable pulse amplitudes 24, which are discussed in more detail below.

Please replace the paragraph beginning on page 25, line 24, with the following rewritten paragraph:

An exemplary configuration for adjustable bias voltage 30 is illustrated in Fig. 8. As shown in Fig. 8, adjustable bias voltage 30 may include transistors 100 and 102 and DAC 106 including resistor 108. Reference voltage V_{ref} may be applied to line 110 passing through resistor 108 to generate bias reference voltage VBIASREF along line 112. The settings of DAC 106 may be used to alter the resistance of resistor 108 and, therefore, may be used to alter bias reference voltage VBIASREF. In general, the settings of DAC 106 may be controlled by data input 82, which may include laser fuses, metal mask options or data transmitted from a magnetic element storage latch arranged within MRAM device 10. Other circuitry other than the one depicted in Fig. 8 may be used to bias voltages applied to magnetic elements of MRAM device 10, depending on the design characteristics of the device. As such, the adjustable bias voltage circuit provided herein is not necessarily restricted to the circuitry illustrated and described in reference to Fig. 8. In other embodiments, the bias voltage circuit provided herein may be omitted from MRAM device 10. In particular, the inclusion of such circuitry is not necessarily needed for the operation of MRAM device 10.

Please replace the paragraph beginning on page 40, line 12, with the following rewritten paragraph:

Figs. 16 and 17 illustrate an exemplary configuration of conductive structures arranged about magnetic elements 220 and 222 which may constitute conductive paths 238 and 240. In particular, Figs. 16 and 17 illustrate schematic views of nonvolatile portion 234 depicting exemplary layouts of structures constituting portions of conductive paths 238 and 240. As shown in Figs. 16 and 17, nonvolatile portion 234 may include conductive structures 250 and 254, vias 252, 256 and 261 and electrodes 258 arranged adjacent to magnetic element 220 and 222. Although Fig. 16 and ~~5~~ 17 illustrate different cross-sectional views for the arrangement of conductive structures 250 and 254, vias 252, 256 and 261, electrodes 258 around magnetic elements 220 and 222, Figs. 16 and 17 are illustrated as schematic drawings and, therefore, do not relate the position of magnetic elements 220 and 222 with respect to those different cross-sectional views. Figs. 16 and 17 are merely illustrated to show exemplary configurations conductive paths 238 and 240 as well as exemplary current paths that may be used when programming and loading data from magnetic elements 220 and 222. In addition, it is noted that margin mode circuit lines MM48 and MM49, transistors Q5 and Q6 and conductive lines 241, described in more detail below, are not shown in Figs. 16 or 17 to simplify the drawings. Such components may be included within the embodiments described in reference to Figs. 16 and 17 or may be omitted from control data latch 170 in some cases.

Please replace the paragraph beginning on page 46, line 10, with the following rewritten paragraph:

Fig. 17 illustrates an exemplary configuration of loading data from magnetic elements 220 and 222. As noted above, a bias voltage may be applied to LOAD line during a loading operation of control data latch 170. Such an application of a bias voltage may activate transistors Q5 and Q6 to enable current flow from nodes 228 and 229 of volatile portion 232 to magnetic elements 220 and 222 in nonvolatile portion 234 as described above in reference to Figs. 14 and 15. In some embodiments, conductive paths 238 may be run to a designated ground line within control data latch 170. In other embodiments, however, conductive paths 328 may be configured to run such a current flow to current source lines 242 and 244 as shown in Fig. 17. In such an embodiment, current source lines 242 and 244 may serve as virtual ground lines during a loading operation of control data latch 170. The use of current source lines 242 and 244 as ground lines may advantageously eliminate the ~~needs~~ need to incorporate a ground line specified for such a use in control data latch 170. In addition, the need to have transistors configured to induce current flow to such a designated ground line may be eliminated. Consequently, the circuitry of control data latch 170 may be simplified and the amount of area it occupies may be reduced relative to embodiments in which a designated ground line and transistors are included.